

REMARKS

Claims 8-21 were examined. Claims 8 and 15 are requested to be amended. These claims have been amended to put them in better condition for allowance and to narrow the issues on Appeal. Accordingly, claims 8-10, 12-17 and 19-21 remain in the application.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attachment is captioned "Version With Markings To Show Changes Made."

I. Claims Rejected Under 35 U.S.C. § 112, second paragraph

Claims 8-21 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Claims 11 and 18 have been cancelled.

In regard to claims 8 and 15, the Examiner states that the grammatical structure of the elements related to the scalability of the first and second dielectric materials is vague and it is not clear if the gate length refers to the feature size technology or to the first and second dielectrical materials. Applicant seeks to amend claims 8 and 15 to more clearly claim the subject matter which Applicant regards as the invention. The claims, as amended, clarify that the first and second dielectric materials are scalable for use with any feature size technology where that feature size technology has a gate length within the range of 25-150 nm. Applicant requests that the amendment be entered because the amendment will narrow issues for consideration on Appeal and put the claims in better condition for allowance. Accordingly, reconsideration and withdrawal of the indefiniteness rejection of claims 8-10, 12-17 and 19-21 are requested.

II. Claims Rejected Under 35 U.S.C. § 103

Claims 8-13 and 15-20 stand rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,963,810 issued to Gardner et al (hereinafter "Gardner") in view of U.S. Patent No. 4,015,281 issued to Nagata, et al. (hereinafter "Nagata") and U.S. Patent No. 5,990,516

issued to Momose, et al. (hereinafter "Momose"). Applicant respectfully disagrees for the following reasons. Claims 11 and 18 have been cancelled.

In order to establish a *prima facie* case of obviousness, the Examiner must show that the cited references, combined, teach or suggest each of the elements of the claim. In regard to claims 8 and 15, these claims include of the elements of the first and second dielectrical materials being scalable for a set of feature size technologies, these feature size technologies being defined by the gate length being in the range of 25-150 nm. The Examiner has failed to indicate any part of the cited references that teaches first and second dielectric materials which are scalable for gate lengths in the full range of 25-150 nm and where the thickness of the first and second materials are determined by the relationship $t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$ as claimed in amended claims 8 and 15. The Examiner relies on Gardner for teaching a gate dielectric layer composed of two separate layers and equates the first dielectric layer to a silicon nitride layer and a second dielectrical layer to a BST layer. However, Gardner clearly states that the range of thickness for the nitride layer is 5-15 Å. See Gardner, col. 6, lines 40-42. This range of thickness for a nitride layer is insufficient to cover the necessary range of thickness for the first dielectrical layer which it is stated to be equivalent to because the first dielectrical layer must have the ability to have a thickness that exceeds 15 Å in order to be characterized as scalable for a set of feature size technologies having a gate length from 25-50 nm and where the first material and second material thicknesses are governed by the stated formula. See also, Table 1, page 11 of the application. Thus, Gardner does not teach a first dielectric layer having the properties claimed in claims 8 and 15.

The Examiner has not indicated any part of Nagata or Momose that teaches or suggests a first and second dielectric layers as claimed in claims 8 and 15. Thus, Nagata and Momose do not cure the defects of Gardner and the combined references do not teach each of the elements of claims 8 and 15. Accordingly, reconsideration and withdrawal of the obviousness rejection of claims 8 and 15 are requested.

In regard to claims 12 and 19, the Examiner has failed to indicate any part of the cited references that teaches or suggests that the first gate dielectric material is selected from one of HfO₂,

ZrO_2 , BaO , La_2O_3 , or Y_2O_3 , as claimed in claims 12 and 19. Thus, the Examiner has failed to establish a *prima facie* case of obviousness for claims 12 and 19. Accordingly, reconsideration and withdrawal of the obviousness rejection of claims 12 and 19 are requested.

In regard to claims 9-10, 13, 16-17 and 20, these claims depend from independent claims 8 and 15 and incorporate the limitations thereof. Thus, at least for the reasons mentioned in regard to claims 8 and 15, these claims are not obvious over the cited references. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

Claims 14 and 21 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Gardner in view of Nagata and Momose and further in view of U.S. Patent No. 5,258,645 issued to Sato (hereinafter "Sato").

Claims 14 and 21 depend from independent claims 8 and 15 and incorporate the limitations thereof. Thus, at least for the reasons mentioned in regard to claims 8 and 15, claims 14 and 21 are not obvious over Gardner in view of Nagata and Momose. Further, Sato does not cure the defects of Gardner. The Examiner has not indicated any part of Sato that teaches or suggests a first and second dielectric material being scalable over a range of gate lengths of 25-150 nm where the thickness of the two dielectric materials are defined by the relationship $t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$.

Therefore, claims 14 and 21 are not obvious over the cited references. Accordingly, reconsideration and withdrawal of the obviousness rejection of claims 14 and 21 are requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, as amended, namely claims 8-10, 12-17, and 19-21 patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207 3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date:

11/13/02

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CERTIFICATE OF TRANSMISSION:

I hereby certify that this paper is being facsimile transmitted to the U.S. Patent and Trademark Office on November 13, 2002.

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE
IN THE CLAIMS**

Please amend the claims as follows:

8. (Five Times Amended) A transistor device having a gate electrode overlying a gate dielectric formed directly on a semiconductor substrate, the gate dielectric comprising:
a first dielectric material having a first dielectric constant; and
a second dielectric material having a second dielectric constant different from the first dielectric constant[; and],
the first and second dielectric materials being scalable for a set of feature size technolog[y]ies,
the set of feature size technologies defined by [having] a gate length in the range of 25-150nm[.],and

wherein the first material thickness and the second material thickness are determined by the relationship

$$\frac{t_1}{k_1} + \frac{t_2}{k_2} = \frac{t_{ox}}{k_{ox}}$$

wherein t_1 is the first material thickness,
 t_2 is the second material thickness,
 t_{ox} is the minimum thickness for a gate dielectric of silicon dioxide for a chosen gate length,
 k_1 is the dielectric constant for the first dielectric material,
 k_2 is the dielectric constant for the second dielectric material, and
 k_{ox} is the dielectric constant of silicon dioxide.

15. (Four Times Amended) An apparatus comprising:

a semiconductor substrate having a transistor device formed thereon, the transistor device having a gate dielectric disposed directly between a surface of the substrate and a gate electrode comprising:

a first dielectric material having a first dielectric constant; and

a second dielectric material having a second dielectric constant different from the first dielectric constant[; and],

the first and second dielectric materials being scalable for [a]each of a plurality of feature size technolog[y]ies, having a gate length in the range of 25-150nm[.], and

wherein the first material thickness and the second material thickness are determined by the relationship

$$\frac{t_1}{k_1} + \frac{t_2}{k_2} = t_{ox}/k_{ox}$$

wherein t_1 is the first material thickness,

t_2 is the second material thickness.

t_{ox} is the minimum thickness for a gate dielectric of silicon dioxide for a chosen gate length.

k_1 is the dielectric constant for the first dielectric material,

k_2 is the dielectric constant for the second dielectric material, and

k_{ox} is the dielectric constant of silicon dioxide.

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